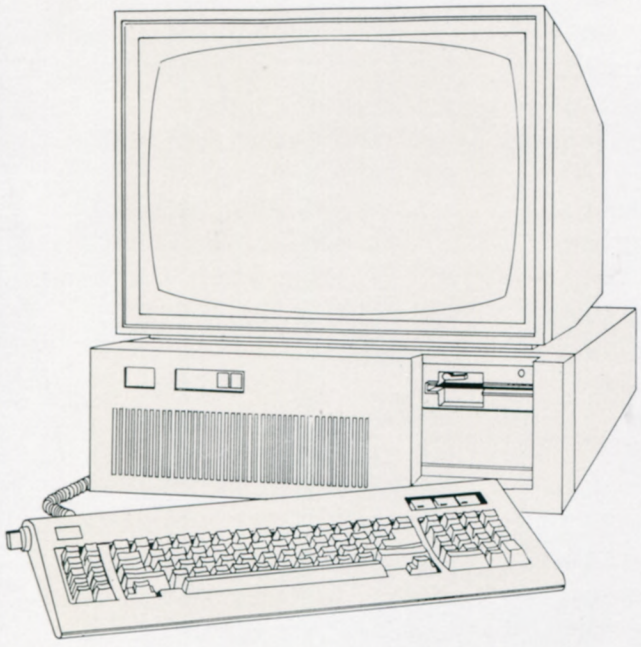
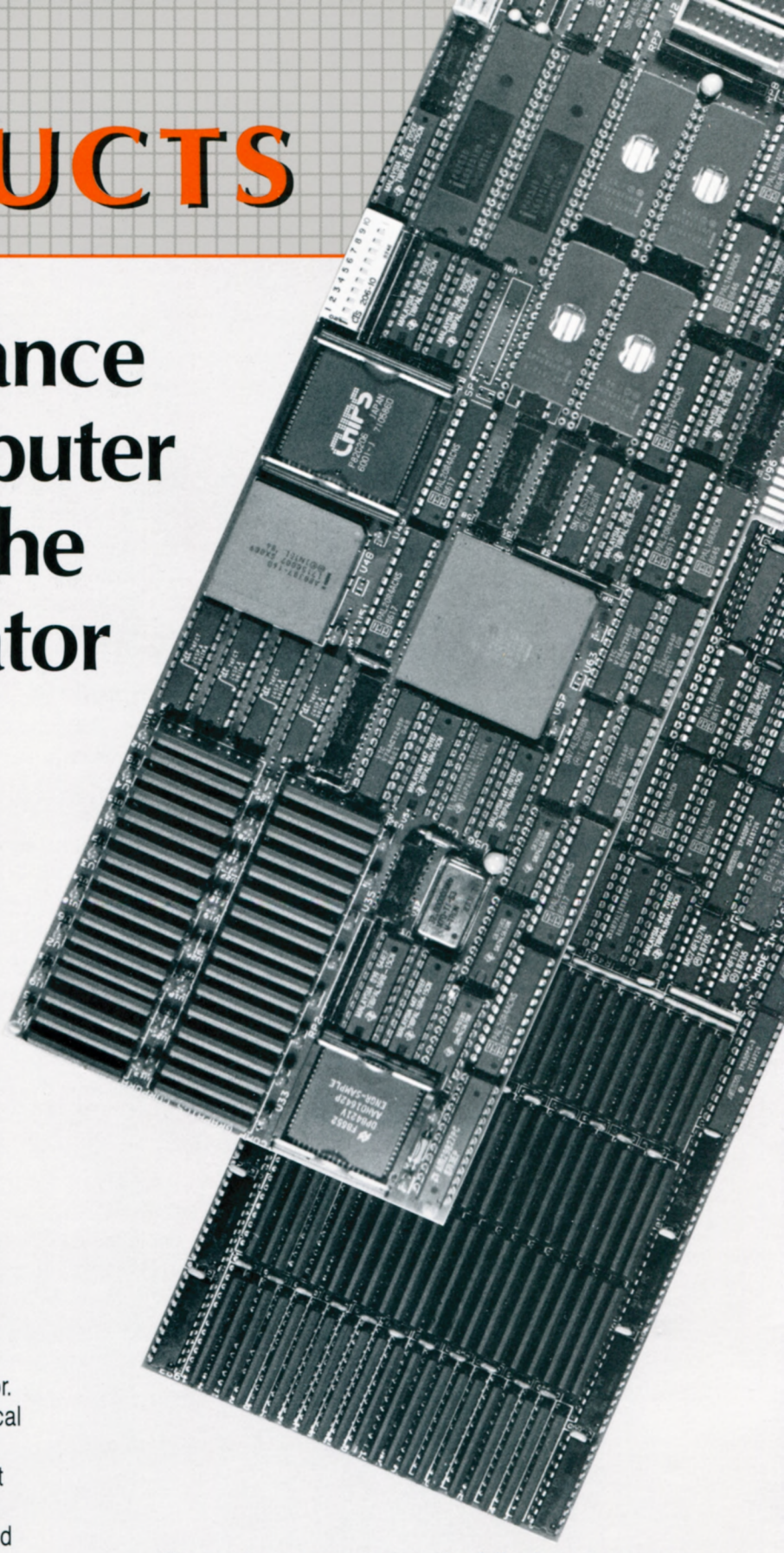
Omnicomp
Graphics Corporation

PC PRODUCTS

High Performance Personal Computer Graphics for the System Integrator





Omnicomp Graphics Corporation designs, manufactures and markets graphics display subsystems and associated products for the OEM and System Integrator. Since 1983, Omnicomp has provided many technological firsts to the computer graphics and System Integrator communities. Included, among those firsts, are the first hardware implementation of GKS (to off-load graphics processing from the host while providing a standardized graphics application interface for systems developers) and the first graphics display subsystem for the advanced MULTIBUS II architecture. Omnicomp continues to provide "Custom Service" to meet the special requirements of its customers.

The products presented on the following pages represent some of Omnicomp's most popular products for the System Integrator using IBM PC's and compatible hosts. For information concerning Omnicomp's other products, please contact your Omnicomp Sales Representative.

Omnicomp
Graphics Corporation

OMNI 1400 GDC

Matchless Graphics for the PC/AT

The OMNI 1400 GDC expands the limits of graphics performance and resolution for the IBM PC/AT and compatibles user. 1280 X 1024 viewable resolution is provided for high performance applications.

The OMNI 1400 GDC provides:

- ❑ Very high speed drawing
- ❑ Hardware cursor
- ❑ Two overlay planes
- ❑ Hardware pan & zoom
- ❑ CGA Feed-through (Optional)
- ❑ 60 Hz non-interlaced display

The OMNI 1400 GDC resides in a single slot of an IBM PC/AT or Compatible, providing a high performance graphics workstation at a competitve price. A 50 pin DIP connector provides I/O with the OMNI 1500 DLP for GKS display list processing.

Resolution

The display memory of the OMNI 1400 GDC is organized as 2048 x 1024 x 8 planes plus 2 overlays, 2048 x 1024 x 4 planes plus 2 overlays or 1024 x 1024 x 8 planes plus 2 overlays. Viewable resolution is software configurable to 1408 x 1024, 1280 x 1024 or 1024 x 768 for either 4 or 8 plane configurations. The visible area may be panned about the total display memory area. The addressable resolution of the 2 overlay planes is always 2048 x 1024.

Color Palette

Palettes of 4096 or 16.7 million colors are available. Either 16 or 256 colors may be displayed depending upon memory configuration. Any color plane may be disabled or made to blink at one of 4 different rates.

Drawing Functions

The drawing functions are performed by a Hitachi Advanced CRT Controller (ACRTC), which executes commonly used functions such as: line, arc, circle, ellipse, rectangle fill, area fill, area copy, etc. In the OMNI 1400 GDC, the ACRTC functions as a dedicated graphics processor closely coupled with multi-ported video memory. This allows drawing operations to be performed continuously.

The ACRTC also provides hardware clipping, zoom and pan.

Cursor

The cursor on the OMNI 1400 GDC is implemented in hardware as a 64 x 64 pixel matrix and/or a full screen crosshair. The cursor can be set to blink on-off or between colors. The cursor may also be positioned with single pixel accuracy at any screen location.

Logical Screen

BASE, UPPER and LOWER screens are fully implemented in the OMNI 1400 GDC. These ACRTC functions allow the three screens to be independently addressed and vertically or horizontally scrolled.

CGA Support

Applications and systems software compatible with the IBM CGA is supported via video feed-through. The video generated by a co-resident CGA is multiplexed with the overlay planes of the OMNI 1400 GDC. The CGA video may be viewed at its normal 320 x 200 (4 color) resolution in the top left corner of the screen or it may be zoomed independently in the X and Y directions. Possible X resolutions are 320, 640, or 1280. Possible Y resolutions are 200, 400, 600 or 800. This allows a single high resolution monitor to meet all user requirements.

Software

A comprehensive library of subroutines are provided with the OMNI 1400 GDC. This library is compatible with FORTRAN and C applications. Advanced software developers have full access to the ACRTC and other hardware features.

Drivers for many popular software products, which benefit from the high performance and resolution of the OMNI 1400 GDC, are currently available or in development. Please contact Omnicomp for current information on supported packages.

Models

Model 64 4 Planes, 2048 x 1024 Addressable Resolution, 2 Overlay Planes. 16 of 4096 Colors.

Model 68 4 Planes, 2048 x 1024 Addressable Resolution, 2 Overlay Planes. 16 of 16.7 Million Colors.

Model 104 8 Planes, 2048 x 1024 Addressable Resolution, 2 Overlay Planes. 256 of 4096 Colors.

Model 104-1 8 Planes, 1024 x 1024 Addressable Resolution, 2 Overlay Planes. 256 of 4096 Colors.

Model 108 8 Planes, 2048 x 1024 Addressable Resolution, 2 Overlay Planes. 256 of 16.7 Million Colors.

Model 108-1 8 Planes, 1024 x 1024 Addressable Resolution, 2 Overlay Planes. 256 of 16.7 Million Colors.

Compatibility

Single card IBM PC/AT or Compatible.

Memory

Display memory is 2.5 megabytes organized as 2048 x 1024 x 8 planes plus 2 overlays, or 1.5 megabytes organized as either 2048 x 1024 x 4 planes plus 2 overlays or 1024 x 1024 x 8 planes plus 2 overlays.

Graphics Controller

The drawing processor is the Hitachi Advanced CRT Controller (ACRTC). The OMNI 1400 GDC occupies 16 bytes of I/O address. The base address is switch selectable.

BUS I/O

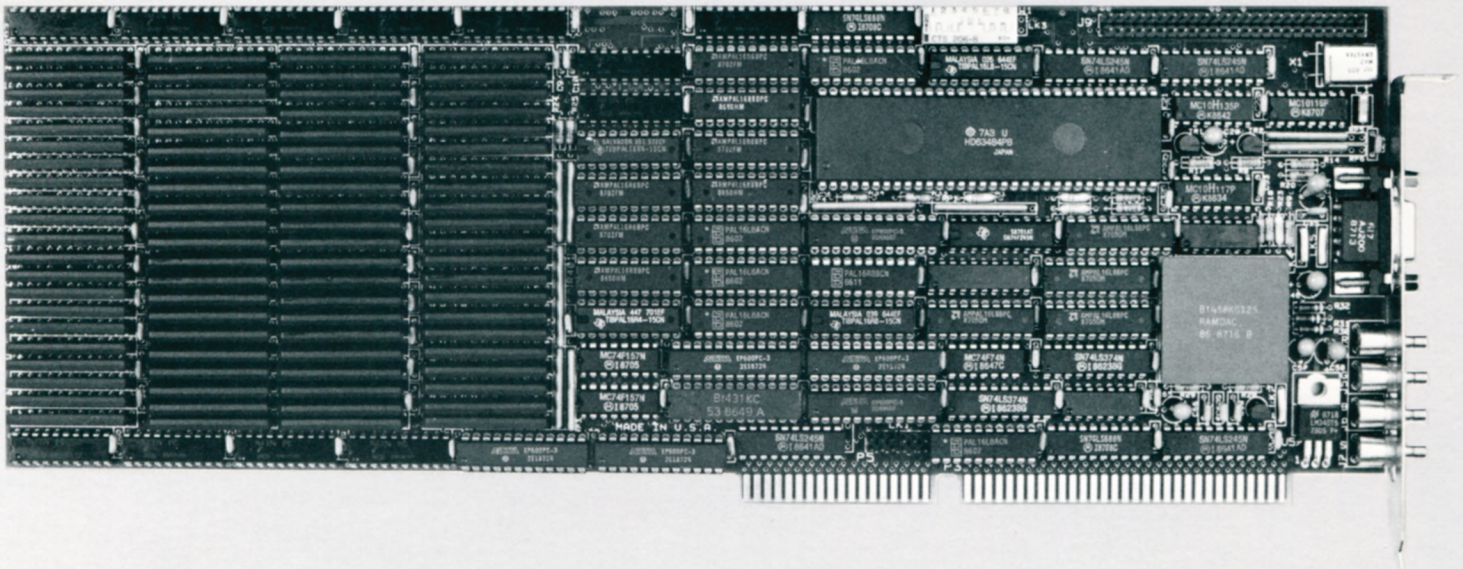
Images from PC Memory to Display Memory - 1.3 MBytes per second using 16 bit I/O.

Drawing Speeds

Line	2 megapixels per second
Circle	1 megapixels per second
Rectangle Fill	2 megapixels per second
Copy	1.3 megapixels per second
Fast Fill	32 megapixels per second

Video Output

Video scan rate is 40 KHz to 64 KHz. Suitable monitors are available from Omnicomp Graphics Corporation.



OMNI 1500 DLP

Extended GKS Display List Processing

High performance GKS display list processing is the primary function of the OMNI 1500 DLP. Utilizing the most recent advances in microprocessor and memory technologies, the OMNI 1500 DLP alleviates the volume of bus traffic and host computation associated with graphics display list processing by providing extended GKS functionality on a single PC/AT add-in circuit card.

The OMNI 1500 DLP can be configured to have one or more companion OMNI 1400 GDCs in an IBM PC/AT or compatible.

The 4 MIP 80386/80387 compute engine of the OMNI 1500 DLP is dedicated to executing Omnicomp's firmware resident GKS commands. Up to four megabytes of on-board, high density dynamic RAM are available for storage of a display list for the co-resident OMNI 1400 GDCs which may be concurrently driven by the OMNI 1500 DLP via a ribbon cable interconnect.

The OMNI 1500 DLP's OMNI*GKS firmware provides application software compatibility with the OMNI 1000 GDC, OMNI 1200 GDC and OMNI 2000 GDM.

Models

Model 01 - 1 Megabyte of 0 Wait State Dynamic RAM.
Model 02 - 2 Megabytes of 0 Wait State Dynamic RAM.
Model 04 - 4 Megabytes of 0 Wait State Dynamic RAM.

Processor

80386 microprocessor (16 MHz)
80387 numeric coprocessor (16 MHz)

Memory

512 Kilobytes of EPROM (A portion of EPROM space is reserved for customer developed firmware.)

1, 2 or 4 Megabytes of DRAM (0 wait state access).

PC/AT Bus Interface

The PC/AT memory is mapped as local memory to the OMNI 1500 DLP processor. The OMNI 1500 DLP is a DMA device to the PC/AT.

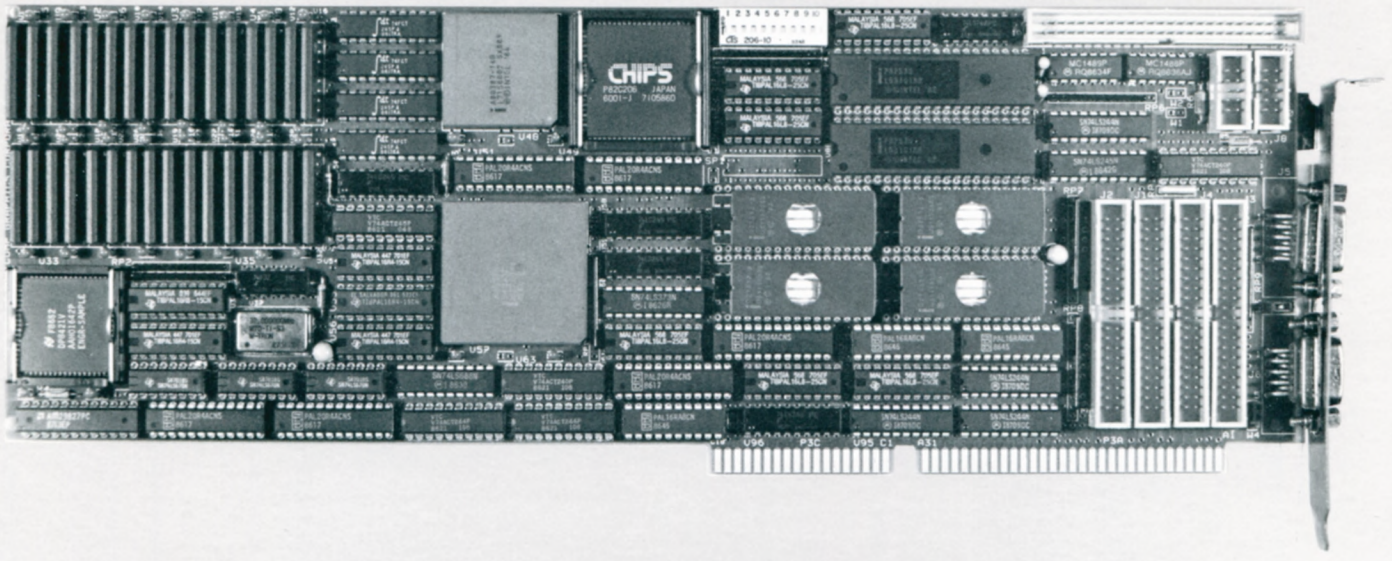
OMNI 1400 GDC Interface

A single 50 line ribbon cable allows connection of multiple OMNI 1400 GDCs to one OMNI 1500 DLP. Each GDC is individually addressed via select lines.

Peripheral Interfaces

A total of 4 RS 232-C serial interfaces are provided on the OMNI 1500 DLP. They may be configured, as needed, for keyboard(s), graphic locator device(s) or host interface.

There are 2 DEC User Peripheral compatible interfaces on the OMNI 1500 DLP. One supports DMA via DR11-W/DRV11-WA. The second provides Programmed I/O via DR11-C/DRV11. They may be used for communications with an external host.

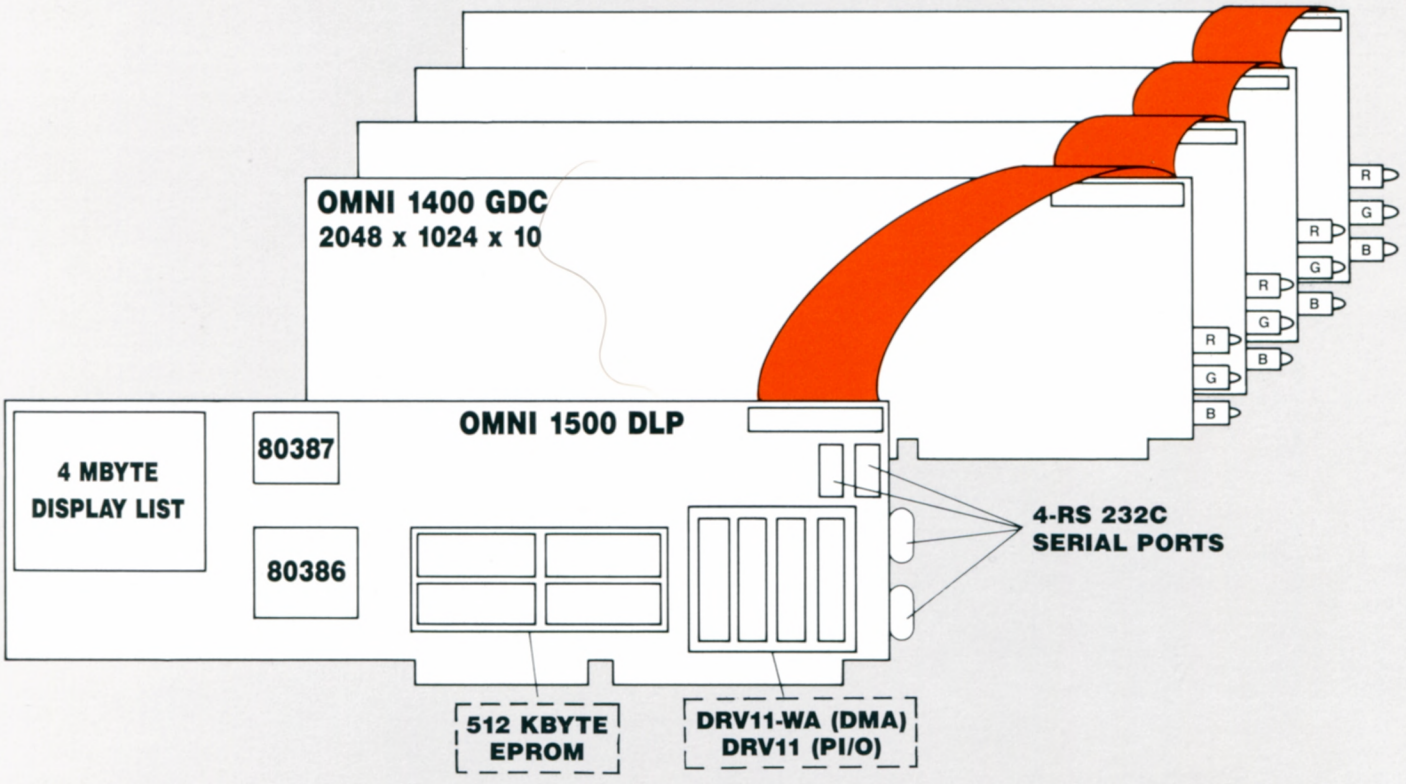


OMNI 1500 GDS

The Graphics Subsytem for High Performance Applications

The OMNI 1500 GDS is configured as one OMNI 1500 DLP and one or more companion OMNI 1400 GDCs that reside in a stand-alone desktop or deskside package (taking power via an AT-like backplane) and communicates with the host via the DR11-W (DMA), DRV11 (PI/O) or serial (RS 232-C) interfaces present on the OMNI 1500 DLP. Inter-module communication is via a bi-directional 16 bit interface located at the top edge of each circuit board.

The OMNI 1500 GDS is a very powerful and flexible graphics solution for the OEM. It is designed to support multiple screen applications, including Process Control/Industrial Automation, Computer Aided Mapping or CAE.



Multiple OMNI 1400 GDC's may be attached to a single OMNI 1500 DLP. OMNI*GKS firmware provides full multichannel workstation display list support.

OMNI 1500 DLP Display List Processor

- ☐ Single Board
- ☐ OMNI*GKS Firmware
- ☐ 80386/80387 Processor
- ☐ DMA and Programmed I/O Parallel Interfaces
- ☐ 4 Serial Interfaces for Keyboards, Mice, etc.
- ☐ PC/AT Compatible

OMNI 1400 GDC Graphics Display Controller

- ☐ Single Board
- ☐ 2048 x 1024 x 8 Resolution
- ☐ Plus 2 Overlay Planes
- ☐ Hardware Cursor, Zoom and Pan
- ☐ 60 Hz Non-interlaced
- ☐ PC/AT Compatible

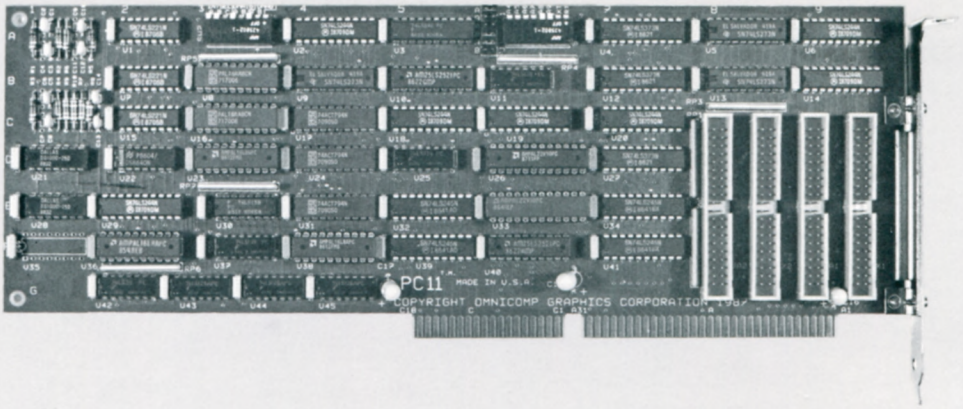
PARALLEL INTERFACE MODULES

Parallel Interface Modules for the IBM PC and PS/2 Families

Omnicomp Graphics Corporation manufactures a series of parallel interface products, for IBM PC/XT/AT and PS/2, which emulate the DEC User Peripheral Interfaces (DR11-W/DRV11-WA and DR11- C/DRV11). These parallel interface products, when installed in an IBM PC compatible or PS/2 host, provide communication with DEC compatible peripherals such as graphics display controllers. Omnicomp also supplies similar parallel interface products for MULTIBUS iSBX and VME.

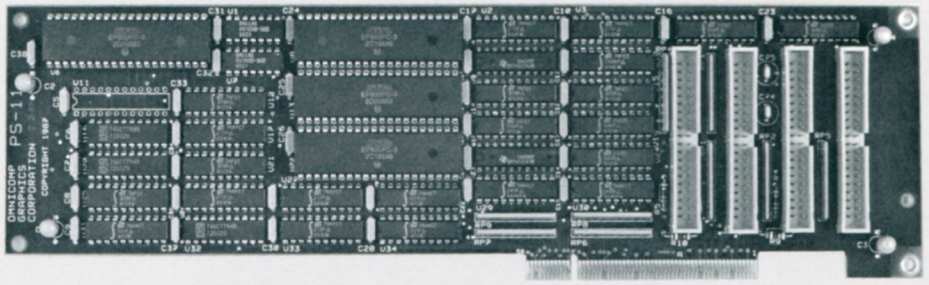
PC11

The PC11 is compatible with the IBM PC/XT/AT/RT. The PC11 emulates either the DRV11-WA (DMA) or the DRV11 (PI/O) host interface. An IBM PC/XT/AT/RT with a PC11 installed may host a peripheral which is compatible with either of these interfaces. All DRV11-WA (DMA) modes are supported through the use of host buffers. PC/RT operation is supported via on-board switching.



PS11

The PS11 is compatible with the IBM PS/2 Micro Channel based computers. The PS11 emulates either the DRV11-WA (DMA) or the DRV11 (PI/O) host interface. An IBM PS/2 with a PS11 installed may host a peripheral which is compatible with either of these interfaces. All DRV11-WA (DMA) modes are supported through the use of host buffers.



Omnicomp™
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Optimizing Computer Graphics . . . by Design.

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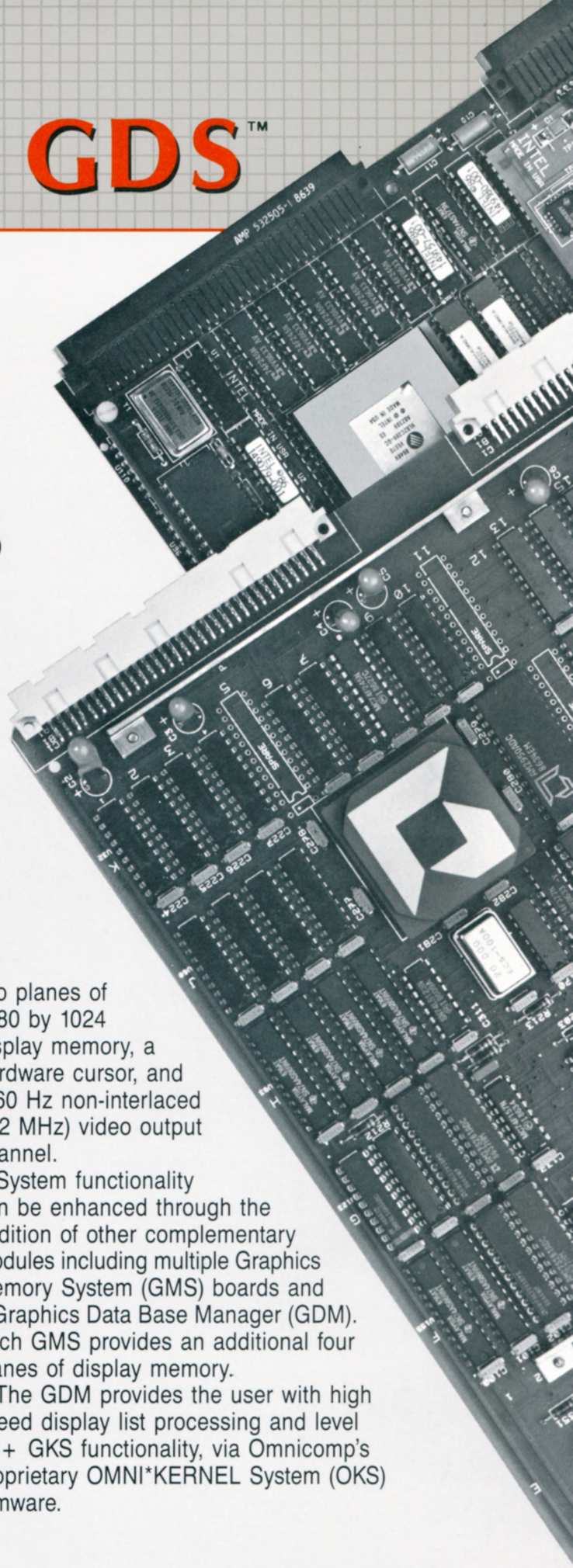
OMNI 2000 GDS™

The High Performance OEM Graphics System



The OMNI 2000 GDS incorporates high performance vector and raster graphics as well as image processing in a single system.

The OMNI 2000 GDS is available as a traditional packaged system with DEC compatible parallel interfaces or as a board level system with an Intel MULTIBUS II system bus interface. By combining sophisticated graphics system design techniques with a high performance public bus structure, the OMNI 2000 GDS provides an opportunity for system developers to integrate high performance vector and image graphics with powerful computing platforms on the same system bus.

The OMNI 2000 GDS is a modular, multiple board system which conforms to the EUROBOARD form factor. Two system interfaces are provided: P1 - the standard iPSB interface using the message passing protocol, and P3 - the interface to the GBX bus, passing control and data signals unique to the OMNI 2000 GDS.

At a minimum, the OMNI 2000 GDS system consists of two modules, the Graphics Control Processor (GCP) and the Graphics Output System (GOS). This configuration provides a six mips bit slice geometry processor, an optional six mflops floating point coprocessor, a proprietary vector coprocessor, a graphic input device controller, two planes of 1280 by 1024 display memory, a hardware cursor, and a 60 Hz non-interlaced (112 MHz) video output channel.

System functionality can be enhanced through the addition of other complementary modules including multiple Graphics Memory System (GMS) boards and a Graphics Data Base Manager (GDM). Each GMS provides an additional four planes of display memory.

The GDM provides the user with high speed display list processing and level 2C+ GKS functionality, via Omnicomp's proprietary OMNI*KERNEL System (OKS) firmware.

Omnicomp
Graphics Corporation

OMNI 2000 GDS™

Graphics Control Processor

The Graphics Control Processor (GCP) is a graphic drawing engine and a geometry processor. All GCP functions are controlled by a six mips AMD 29116 based bit slice processor which uses an 88 bit wide micro-word instruction. An optional six mflops floating point coprocessor, the AMD 29325 floating point ALU, communicates with the bit slice processor through a dual ported 8 KByte scratch RAM.

The bit slice processor provides significant flexibility in the application functionality of the OMNI 2000 GDS. This processing power is easily applied to both geometry processing and digital filtering. The design of the microcode takes full advantage of this resource by providing commands for two and three dimensional vector, two dimensional polygon oriented functions, and image analysis and processing operations. In addition to vector and polygon draw, transform, and zoom operations, a convolution function provides digital image filters including Laplace, high, and low pass. The GCP communicates with the host CPU through DEC compatible parallel interfaces or through the iPSB interface. Efficient data transmission is maintained with both data channels by using buffered fifo's. Also included within the GCP module is a peripheral coprocessor which supports four RS-232 serial data ports. This Intel 80188 based coprocessor provides a direct link between a locator device, such as a mouse or digitizer, and the cursor hardware. This offloads the cursor positioning responsibilities from the drawing engine.

For applications which require a variety of rapidly generated bit mapped text fonts, the GCP contains 10 KBytes of high speed memory which may be downloaded with custom text fonts. A typical 15 pixel wide by 20 pixel high bit mapped text character is drawn in less than ten microseconds. Bit mapped text may be clipped, pixel by pixel, to an arbitrary screen viewport with no performance penalty.

The primary function of the GCP is to execute drawing and image manipulation commands which are passed to it either by the GDM or by the host CPU. The GCP is capable of processing drawing primitives specified in both screen and world coordinate systems. Those drawing primitives which are specified in the world coordinate system are first converted to screen coordinates by the floating point coprocessor. The conversion process consists of a general geometric transformation, followed by a clipping operation and finally a window to viewport mapping. The bit slice processor converts screen coordinate drawing primitives and raster image data into a series of data words and control signals used by the vector coprocessor.

The 12 MHz vector coprocessor utilizes proprietary logic developed by Omnicomp Graphics Corporation. This coprocessor is capable of generating vectors of any orientation at the rate of one pixel per 80 ns as well as initiating the frame buffer write operation in parallel with the geometry processor.

In order to decouple the vector coprocessor from the system frame buffer, a 20 pixel cache is employed. The pixel cache is organized as a 5 pixel by 4 pixel array. The entire contents of the pixel cache can be written to an arbitrary location within the frame buffer in a single frame buffer memory cycle of 500 ns.

Because of the 5 by 4 pixel cache and the proprietary vector coprocessor, the

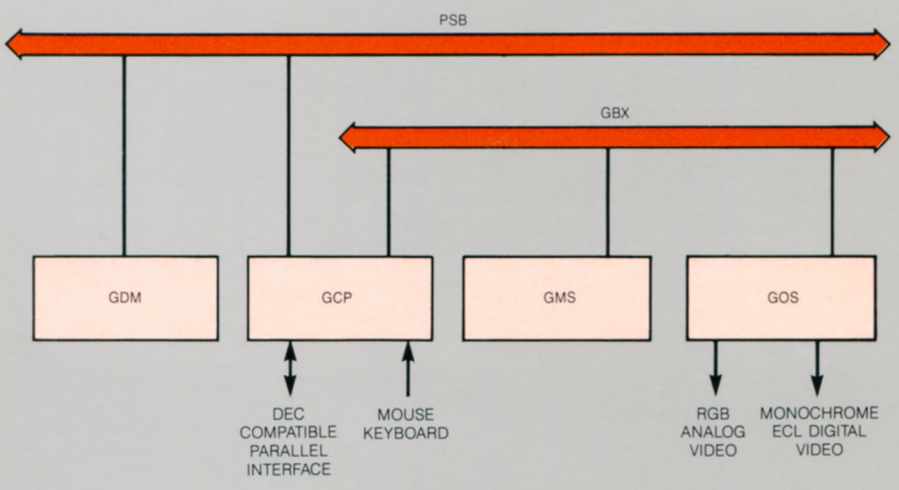
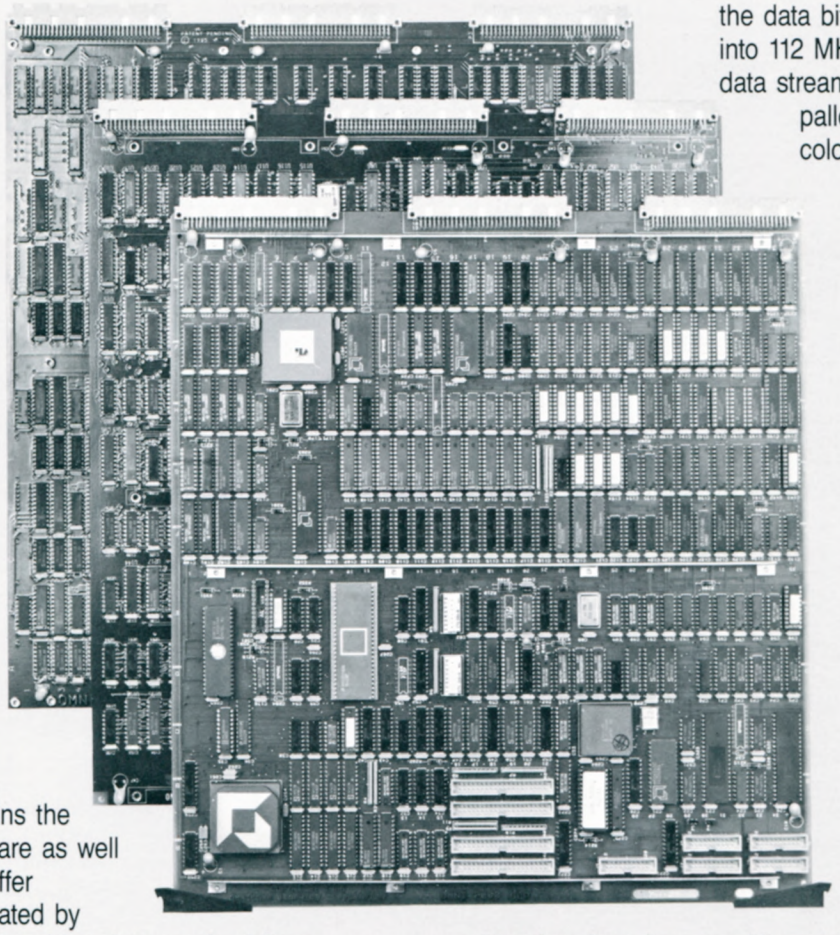


Figure 1: The OMNI 2000 GDS system consists of a minimum of two modules: the graphics control processor (GCP) and the graphics output system (GOS) module. Added functionality can be obtained by using a graphics memory system (GMS) module and a graphics database manager (GDM).

OMNI 2000 GDS can sustain a throughput of over 200,000 random forty pixel vectors per second. This unique architecture minimizes the number of frame buffer accesses required for typical drawing operations and facilitates highly efficient execution of all graphic primitives. Fat lines, patterned fills, patterned lines, irregular fills, polymarkers, bit mapped text and paint brush style strokes are examples of operations which benefit from this drawing efficiency.



Graphics Output System

The GOS module contains the frame buffer control hardware as well as two planes of frame buffer memory. Video data generated by these planes can overlay the video data received from the optional GMS modules or be used as a two plane frame buffer in a stand-alone configuration. The GOS multiplexes the data bits it receives from the GMS into 112 MHz video signal. The video data stream is then routed to the color pallettes, which provide the color look up and digital to analog signal conversion functions. When configured with two GMS boards, the OMNI 2000 GDS provides 256 displayable colors from a palette of 16.7 million colors. A separate overlay color look up table is used to control how the overlay video data and the hardware cursor from the GOS affect the primary video signal. Systems configured without a GMS module use the GOS frame buffer to provide either a double buffered monochrome or four color display. In addition, the GOS provides a digital ECL video interface for use with monochrome monitors.

In order to simplify the use of the graphic cursor, the GOS provides both hardware generated matrix and crosshair

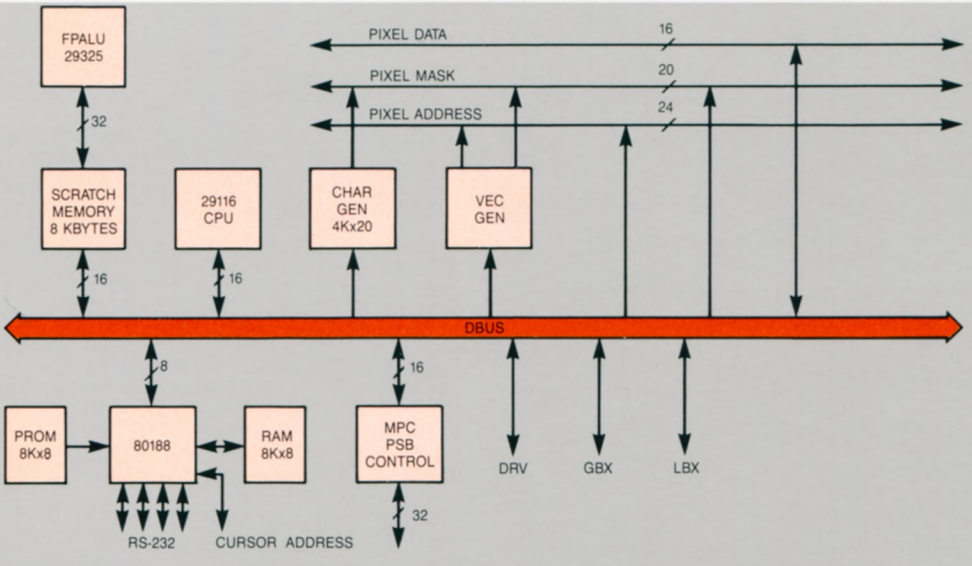


Figure 2: All GCP functions are controlled by an AMD 29116-based bit-slice processor. The GCP communicates with the host through either a DEC-compatible interface or the MULTIBUS II's iPSB.

Figure 3: If each pixel in the vector represented in (A) were drawn individually, 15 memory cycles would be required. By allowing simultaneous access of the two-dimensional regions of the frame buffer, only three memory cycles are required. If the text character represented in (B) were drawn using a pixel block transfer, a frame buffer that allows only scan-line access would require 12 memory cycles to complete the transfer, the GDS requires only six memory cycles.

cursors. By generating the graphic cursor on the fly rather than by drawing it into a frame buffer plane, any interference between frame buffer data and the cursor is removed. The cursor video signal is routed through the overlay look up table to allow the cursor display characteristics to be adjusted.

Graphics Memory System

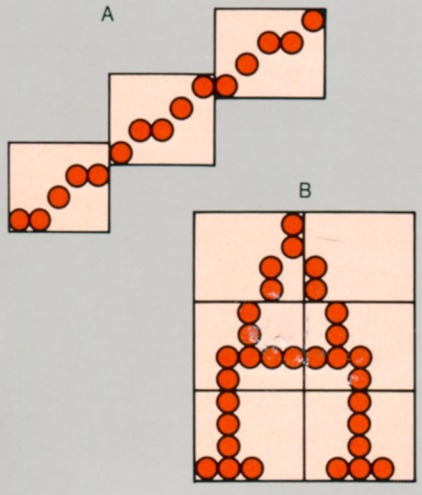
The Graphic Memory System (GMS) modules provide up to 1280 x 1024 x 8 frame buffer memory (double buffered) in multiple configurations. By employing dual ported video RAM in the GMS design rather than conventional DRAM, a more efficient frame buffer memory organization is made possible. Traditional frame buffer designs force the frame buffer word to be a one dimensional group of pixels which fall on a single scan line. Because the video output data is read from the frame buffer one scan line at a time, this organization maximizes the video output bandwidth of the frame buffer memory. However, scan line organization of the frame buffer memory significantly reduces the frame buffer bandwidth.

The frame buffer implementation, used by the OMNI 2000 GDS maximizes the frame buffer input bandwidth and allows multiple scan lines to be accessed simultaneously. Most drawing operations execute with fewer frame buffer accesses when small two dimensional regions of the frame buffer are accessed at once rather than by a single scan line. The OMNI 2000 GDS frame buffer memory is organized as 256 rows by 256 columns of 5 pixel by 4 pixel blocks. This memory organization is possible due to the dual ported video RAM's high serial output port bandwidth, which allows a narrow frame buffer block to provide the required frame buffer output bandwidth.

Physically, each 5 by 4 pixel block consists of 20 pixels which share a common memory address. In order to further reduce the number of frame buffer accesses, the frame buffer design allows the contents of the pixel cache to be written to any location within the frame buffer in a single memory cycle, without regard to the physical frame buffer boundaries. Each pixel within the frame buffer cell is individually addressable. A two-dimensional barrel shifter is used to compensate for misalignment between the contents of the pixel cache and the fixed cell boundaries of the frame buffer.

Serial Versus Parallel

Another form of block pixel transfer is used by the GMS to transfer data from one set of frame buffer planes to another, thus providing a serial double buffering capability. Double buffering is used to delay the visual effects of drawing operations until the drawing is complete. Serial double buffering, as it is employed by the OMNI 2000 GDS, is often significantly more efficient than the traditional parallel double buffering method. The parallel double buffer employs two identical buffers. As one buffer is accessed by the drawing processor, the other buffer is displayed. When the drawing is complete the original drawing buffer becomes the display buffer, and the original display buffer becomes the current drawing buffer. The parallel double buffer is convenient if the



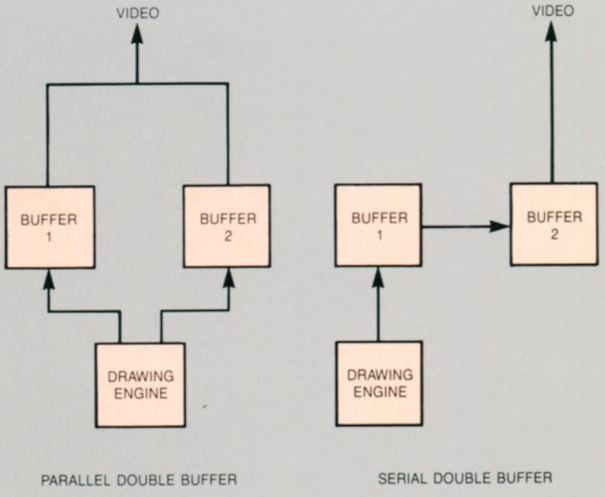


Figure 4: Serial double buffering is often more efficient than the traditional parallel double buffering method. The parallel double buffer uses two identical buffers—as one buffer is accessed by the drawing processor, the other buffer is displayed. A serial double buffer dedicates one buffer as a drawing buffer and another as a display buffer.

entire buffer content is regenerated before each buffer swap. If, on the other hand, only a portion of the buffer content is modified, such as in a multiple window display, the parallel double buffer is much less convenient. Because the most recent modifications to the display buffer are not reflected in the current drawing buffer, they must be duplicated in the drawing buffer before the current drawing activity may proceed. This redundant activity significantly affects both system performance and operating overhead.

A serial double buffer on the other hand dedicates one buffer as a drawing buffer and another as a display buffer. As a drawing is completed the contents of the drawing buffer are transferred into the display buffer. The OMNI 2000 GDS performs this block transfer in a single video frame time of 16.667 milliseconds. Each pixel is moved from the drawing buffer to the display buffer just after the display pixel is sent to the screen. This results in an apparently instant change in the display. By employing a dedicated drawing buffer, the inefficiencies of the traditional double buffering method are removed.

Graphics Database Manager

The GDM module is an Intel 80386/80387 based CPU and memory board and is configured as a back-end processor. This allows the bit slice drawing processor to scan the incoming command stream and execute any commands targeted for it. The GDM connects to other system modules via the iPSB bus interface. A 64 Kbyte memory cache is used to allow the 80386/80387 to run at 20 MHz with no wait states. A large display list store, consisting of up to 16 Mbytes of memory, is connected directly to the 32 bit wide memory cache.

The display list operations executed by the GDM correspond directly to standard host based GKS subroutine calls. By using the same OMNI*KERNEL System firmware as other Omnicomp products, the philosophy of providing upward compatibility throughout its family of graphics systems has been retained. Thus, the systems integrator has a price/performance range of software compatible graphics devices with which to address his marketplace requirements. This firmware is written entirely in 80386 assembly language and executes in a stand alone fashion, with no intervening operating system. The responsibilities of the GDM are to manage the data base and graphic attribute control functions.

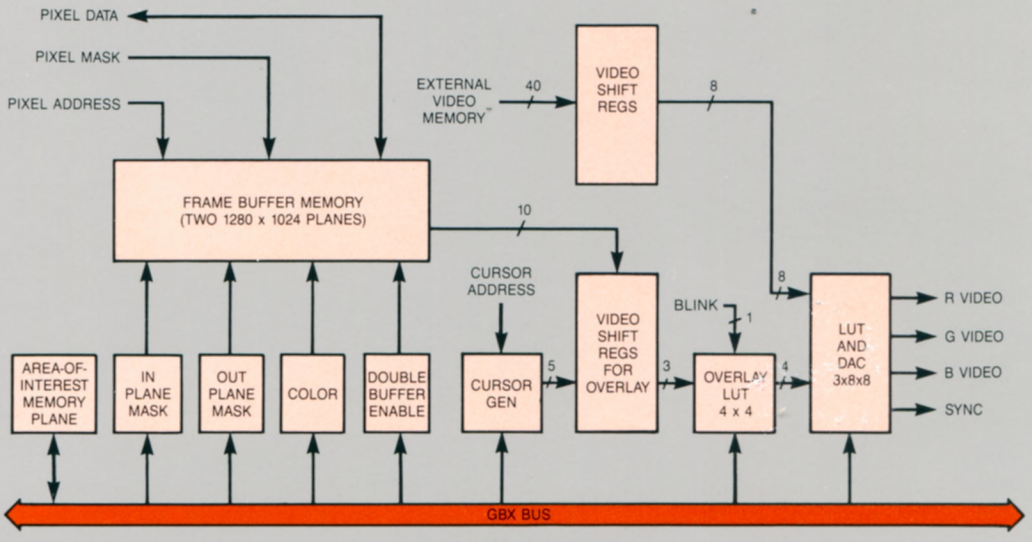


Figure 5: The graphics output system (GOS) module contains two planes of frame buffer memory, an overlay look-up table and a digital ECL video interface. Systems configured without a graphics memory system (GMS) module use the GOS frame buffer to provide either a double buffered monochrome or four-color display.

Designed for the OEM

The modular nature of the OMNI 2000 GDS allows system expansion and enhancement to occur in an incremental manner. The overall design philosophy behind the OMNI 2000 GDS is to provide a family of board level components which may be combined to provide a standard set of high performance graphic display functions.

Graphics display subsystems must be designed to meet the widely varying requirements of OEM's and system integrators. Modular flexibility allows those requirements to be met without the customer purchasing more features than necessary. A modular design also enables the manufacturing company to evolve the subsystem; incorporating new semiconductor innovations, keeping it price/performance competitive. The OMNI 2000 GDS was designed to meet the needs of a broad spectrum of applications. As such, it will remain both a physical product and a design concept. As it evolves over the coming years, most of the currently used components will be designed out in favor of parts providing denser integration, more performance and better economics. What will remain is the concept of what its functionality must be, the algorithms used to provide that functionality and the buses and pathways linking all of its parts internally and externally.

Features

- ☐ Modular Configurations
- ☐ MULTIBUS II iPSB and DR11-W Interfaces
- ☐ High Speed 2D and 3D Geometry Processing
- ☐ Display List Processor via GDM and OMNI*KERNEL System
- ☐ Parallel, Pipelined Architecture
- ☐ Non-destructive Overlay Planes
- ☐ Serial Double Buffering
- ☐ Image Processing Commands
- ☐ Monochrome to 8 Bit Color Planes, Double Buffered
- ☐ Fast Pixel Draws:
  Vectors: Up to 10 Megapixels per Second
  Fills: Up to 40 Megapixels per Second
  BLT: 20 Megapixels per Second
- ☐ High Speed Bit-Mapped Characters (100K Characters per Second)
- ☐ Hardware Screen Clipping
- ☐ Hardware Matrix and Crosshair Cursors

Specifications:

Display Characteristics:
1280 x 1024 Display Resolution
60 Hz Non-interlaced or 30 Hz Interlaced
RS-343 RGB
Pixel Clock: 112 MHz Non-Interlaced
56 MHz Interlaced

Display Memory Configurations:
2 Planes
4 Planes + 2 Overlays
8 Planes + 2 Overlays
4 Planes Double Buffered + 2 Overlays
8 Planes Double Buffered + 2 Overlays

Multiple Processors:
GCP: Geometry Processor - AMD 29116 Bit Slice
Optional Floating Point Coprocessor - AMD 29325 FPP
Vector Coprocessor - Proprietary Logic
Peripheral Coprocessor - Intel 80188

GDM: Display List Processor - Intel 80386
Floating Point Coprocessor - Intel 80387
DIsplay List Memory: 1, 4, 8 or 16 Mbytes

Power Requirements:
250 Watts @ 110 VAC - Typical

Host Interfaces:
MULTIBUS II iPSB
16-Bit Parallel DMA or PI/O
(DRV11-WA/DR11-W or DRV11/DR11-C)

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